Confirmation No. 6084

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellant:	SURDEANU *et al.*	Examiner:	Lin, J.
Serial No.:	10/550,741	Group Art Unit:	2815
Filed:	September 22, 2005	Docket No.:	NL030347 US1 (NXPS.279PA)
Title:	GATE ELECTRODE FOR SEMICONDUCTOR DEVICES		

APPEAL BRIEF

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Dear Sir:

This Appeal Brief is submitted pursuant to 37 C.F.R. §41.37, in support of the Notice of Appeal filed March 10, 2010 and in response to the rejections of claims 6-14 and 17-24 as set forth in the Final Office Action dated December 11, 2009.

Please charge Deposit Account No. 50-4019 (NL030347US1) $670.00 for filing this brief in support of an appeal as set forth in 37 C.F.R. §1.17(c), plus the one month extension fee. If necessary, authority is given to charge/credit Deposit Account 50-4019 additional fees/overages in support of this filing.

I. Real Party In Interest

The real party in interest is NXP Semiconductors. The application is presently assigned of record, at reel/frame nos. 019719/0843 to NXP, B.V., headquartered in Eindhoven, the Netherlands.

II. Related Appeals and Interferences

While Appellant is aware of other pending applications owned by the above-identified Assignee, Appellant is unaware of any related appeals, interferences or judicial proceedings that would have a bearing on the Board's decision in the instant appeal.

III. Status of Claims

Claims 6-14 and 17-24 stand rejected and are presented for appeal. Claims 1-5 and 15-16 are cancelled. A complete listing of the claims under appeal is provided in an Appendix to this Brief.

IV. Status of Amendments

An amendment to the Final Office Action dated December 11, 2009 was filed on February 9, 2010. The Advisory Action dated March 4, 2010 indicates this amendment was not entered. No further amendments have been filed.

V. Summary of Claimed Subject Matter

As required by 37 C.F.R. § 41.37(c)(1)(v), a concise explanation of the subject matter defined in the independent claims involved in the appeal is provided herein. Appellant notes that representative subject matter is identified for these claims; however, the abundance of supporting subject matter in the application prohibits identifying all textual and diagrammatic references to each claimed recitation. Appellant thus submits that other application subject matter, which supports the claims but is not specifically identified above, may be found elsewhere in the application. Appellant further notes that this summary does not provide an exhaustive or exclusive view of the present subject matter, and Appellant refers to the appended claims and their legal equivalents for a complete statement of the invention.

Commensurate with independent claim 6, an example embodiment of the present invention is directed to an MIS type semiconductor device. The device includes a semiconductor substrate (*see, e.g.*, Figures 1-2, reference 2) and a gate electrode (*see, e.g.*, page 4:3-4) formed on a gate insulating film (*see, e.g.*, Figure 2, reference 4 and page 4:3-4) and formed of a gate material (*see, e.g.*, page 7:21-25). The gate electrode comprises a first layer of activated crystalline gate material having a first side oriented towards the substrate and in contact with the gate insulating film (*see, e.g.*, Figure 2, reference 10, and page 7: 3-9). A second side oriented away from the substrate and a grain size (*see e.g.*, Figure 2 and page 3:34-4:1). The first layer of activated crystalline gate material having a doping level of 10^{19} ions/cm^3 or higher (*see, e.g.*, Figure 3 and page 7:10-20). A second layer of gate material is in contact with the first layer of activated crystalline material at the second side of the first layer of activated crystalline gate material, the second layer of gate material having a grain size (*see, e.g.*, Figure 2, reference 16 and page 7:23-28). The grain size of the second layer of gate material is at least twice as large as the grain size of the first layer of activated crystalline gate material (*see, e.g.*, page 3:34-4:2).

Commensurate with independent claim 24, an example embodiment of the present invention is directed to an MIS type semiconductor device. The device includes a semiconductor substrate (*see, e.g.*, Figures 1-2, reference 2), a gate insulating film formed on the substrate (*see, e.g.*, Figure 2, reference 2 and page 4:3-4) and a gate electrode formed on the gate insulating film (*see, e.g.*, Figure 2 and page 4:3-4). The gate electrode includes a first layer of activated crystalline gate material having a first side oriented towards the substrate and in contact with the gate insulating film (*see, e.g.*, Figure 2, reference 10, and page 7: 3-9), a second side oriented way from the substrate (*see e.g.*, Figure 2 and page 3:34-4:1) and a grain size of less than about 5 nm (*see, e.g.*, page 4:1), the first layer of activated crystalline gate material having a doping level of 10^{19} ions/cm^3 or higher (*see, e.g.*, Figure 3 and page 7:10-20). A second layer of gate material in contact with the first layer of activated crystalline gate material at the second side of the first layer of activated crystalline gate material (*see, e.g.*, Figure 2, reference 16 and page 7:23-28), the second layer of gate material having a grain size of less than about 40 nm (*see, e.g.*, Page 3:34). The grain size of the first

layer of activated crystalline gate material is smaller than the grain size of the second layer of gate material (*see, e.g.*, page 3:34-4:2).

VI. Grounds of Rejection to be Reviewed Upon Appeal

The grounds of rejection to be reviewed on appeal are as follows:

A. Claims 6-7, 10-14, 17 and 20-24 stand rejected under 35 U.S.C. § 103(a) over Rhee (U.S. Patent No. 6,667,525) in view of Suguro (U.S. Patent Pub. 2001/0039107) and further in view of Tao (U.S. Patent No. 6,399,515).

B. Claims 8 and 18-19 stand rejected under 35 U.S.C. § 103(a) over the '525, '107 and '515 references in view of Holloway (U.S. Patent No. 6,222,251).

C. Claim 9 stands rejected under 35 U.S.C. § 103(a) over the '525, '107 and '515 references in view of Gardner (U.S. Patent No. 6,160,300)

VII. Argument

A. The Rejection Of Claims 6-7, 10-14, 17 And 20-24 Is Improperly Based On Piecemeal Teachings of The Asserted References

Appellant respectfully traverses the § 103(a) rejection of claims 6-14 and 17-24 because the Examiner's rejection fails to provide a valid reason for the proposed combination of the asserted references. Consistent with M.P.E.P. § 2143.01 and relevant case law, a § 103 rejection must provide evidence of motivation where a proposed combination of references would modify a primary reference. *See, e.g., KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1741 (U.S. 2007) ("A patent composed of several elements is not proved obvious merely by demonstrating that each element was, independently, known in the prior art."). In this instance, the Examiner's rejection proposes to combine the grain sizes of metal gate electrode 3 of the '107 reference with the semiconductor gate layers 23 and 24 of the '525 reference "to reduce the variations in threshold voltage." However, as discussed below, metallic and polysilicon materials exhibit different semiconductor properties that cannot be combined as proposed without extensive modification, beyond that taught in the asserted references. In light of these differences, the proposed combination lacks any supporting evidence, and further does not provide a clearly-articulated reason (or explanation as to how the '525 reference could

or would operate as modified), that would be consistent with the *KSR* decision. Accordingly, the § 103(a) rejection is improper for lack of motivation and Appellant requests that the rejections be overruled.

More specifically, the Examiner's rejection does not provide any support or reasoning for the conclusion that grain size of polysilicon will exhibit semiconductor properties expected as grain sizes used in connection with metallic compounds. Appellant asserts that the teaching of grain sizes in the '107 reference is inextricably linked to the metallic gate material used. The rejection ignores differences in the physical properties of silicon and metal semiconductor material known in the art. For example, as discussed in the '107 reference, metal gate electrodes have reduced resistance (*see* paragraph 0017), and replacing polysilicon gate electrodes with metalized gate electrodes introduces several problems such as an undesirable work function because "metal gate electrodes have a property that the work function of a metal varies as their material varies with crystal orientations." *See, e.g.,* paragraph 0078. Because of these differences, extensive modification to the cited teachings of the '525 and '107 references would be required to overcome various problems associated with metallic gates as discussed above. In view of the above, adequate support for the propose combination has not been presented and Appellant requests the §103 rejections be withdrawn.

In violation of M.P.E.P. § 707.07(f), among other guidelines and laws, the Examiner has chosen not to respond to Appellant's efforts to explain this deficiency. For example, neither the Examiner's response to arguments in the Final Office Action dated December 11, 2009 nor the Advisory Action of March 4, 2010 addresses the differences between these components. Accordingly, the record is insufficient to support or otherwise maintain the rejection as being proper under § 103(a).

With respect to the comments in the Examiner's Advisory Action dated March 4, 2010 (which attempt to buttress the rejection at issue), the Examiner asserts one "would be motivated by the disclosure of [the secondary '107 reference] to combine it with [the primary '525 reference] because of the advantage of having the difference in grain sizes." The Examiner does not explain any such advantage realized apart from that which is explained in Appellant's Specification. The Examiner has apparently recognized that the secondary '107

reference is directed specifically towards metal electrodes and, rather than addressing the recognized incongruent disparities between silicon and metal, such as discussed above, the Examiner improperly generalizes the teachings of the secondary '107 reference to include anything having a grain size. However, the asserted teachings of the secondary '107 reference cannot be combined with the primary '525 reference while ignoring the other teachings of the secondary '107 reference, specifically the teaching of a metal gate electrode. For example, the Examiner has not provided any explanation as to why the metal grain size of the secondary '107 reference would be viewed as being relevant to activated silicon gate material. In doing so the Examiner ignores the physical properties of silicon and metal semiconductor material known in the art, and aspects of the secondary '107 reference regarding the gate material being metal and the physical properties of the metal electrode. Therefore, the Examiner has failed to consider the secondary '107 reference as a whole as required by M.P.E.P. § 2142.02.

By failing to provide any explanation as to how or why the properties of a metal gate electrode have any relevance to a silicon activated region, the Examiner fails to comply with M.P.E.P. § 2142.02 because considering the secondary '107 reference in its entirety, including its teachings regarding the inferior attributes of metal-based grains relative to polysilicon-based grain (see '107 reference at paragraph 0078), the secondary '107 reference expressly teaches away from replacing the polysilicon-based grains with metal-based grains to achieve the relative grain size as set forth in Appellant's claims. According to M.P.E.P. § 2142.02 a "[p]rior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention." Therefore, under M.P.E.P. § 2142.02, the Examiner's rejection fails.

As the asserted combination attempts to focus on individual elements without consideration of the context in which these elements are discussed, the Examiner has failed to consider the cited references "as a whole" and in particular, that the only evidence of record alleged to correspond to the particular grain sizes is that of the secondary '107 reference. As indicated above, this secondary reference teaches away from the combination proposed by the Examiner's rejection. The Examiner attempts to sidestep this issue by isolating teachings relating to grain size and rebuilding anew is clearly improper hindsight.

This improper approach has been addressed, perhaps most authoritatively, by the U.S. Supreme Court's *KSR* decision which states, in pertinent part:

> Although common sense directs one to look with care at a patent application that claims as innovation the combination of two known devices according to their established functions, it can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does. This is so because inventions in most, if not all, instances rely upon building blocks long since uncovered, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known.

KSR Int'l Co. v. Teleflex, Inc., 550 U.S. 398, 418-419 (US 2007) (emphasis added).

Without a proper reason to combine the references in the record, the rejection cannot stand. Accordingly, the § 103(a) rejections are improper and should be withdrawn.

Accordingly, the record contains no explanation or suggestion for why one of ordinary skill in the art would view teachings relating to a metal gate electrode as being relevant to activated silicon gate materials. While the Examiner's rejection attempts to argue that the replacement of the grain (and grain size) taught in the primary '525 reference would somehow achieve a reduction of variation in threshold voltage, the Examiner's rejection fails to account for the evidence of record, in the very same references asserted, that explains the significant problems with such incompatible materials and, therefore, why the skilled artisan would not be motivated to modify the primary '525 reference as asserted. Not only does the Examiner fails to provide an explanation in support, the Examiner's asserted references teach away.

Accordingly, the § 103(a) rejection of claims 6-7, 10-14, 17 and 20-24 is improper and Appellant requests that the rejection be reversed.

B. The Rejection Of Claims 8 And 18-19 Is Improper.

1. The Proposed Combination Of References Lacks Correspondence.

The § 103(a) rejection of claims 8 and 18-19 is improper because none of the cited references teach or suggest the abruptness of the doping profile as claimed. The Examiner improperly asserts that the abruptness of the doping concentration is simply a recognized parameter despite no mention therefore in any of the references. The Examiner's asserted teachings rely upon a general discussion of doping profiles and doping concentration. Accordingly, there is no direction or identification of the abruptness of the doping profile in the cited references.

In order for a parameter to be a result effective variable, a parameter must have been recognized as being relevant to a particular result and have some suggestion to adjust the parameter in a workable range. M.P.E.P. § 2144.05(II)(B) ("A particular parameter must first be recognized as a result-effective variable, i.e., a variable which achieves a recognized result, before the determination of the optimum or workable ranges of said variable might be characterized as routine experimentation."). None of the cited references has been shown to teach the abruptness of the doping profile because the teachings are relatively general and relate simply to the overall doping level, such as optimization for conductivity. *See, e.g.*, Col. 1:38-41. Accordingly, the record does not support that abruptness of the doping profile is a parameter that provides a recognized result.

In further support of the lack of suggestion to experiment with the abruptness of the doping profile, Appellant notes that none of the cited references consider problems of the penetration of dopants from the gate into the gate insulator and channel regions during implantation and dopant activation, which results in decreased performance, as discussed throughout Appellant's specification. As further evidence, the '525 reference and the '107 reference also discuss problems with dopant penetration. *See, e.g.*, Col. 2:5-11 of the '525 reference ("...boron defuses into the semiconductor substrate...") and paragraphs 0022-0026 of the '107 reference ("impurities ...penetrate through the gate oxide into the silicon substrate"). Accordingly, the evidence of record would have led the skilled artisan away from modifications relating to the abruptness of doping profiles.

2. The § 103(a) Rejections of Claims 8, 18-19 Are Improper Because The Examiner's Reliance On The '251 reference Does Not Overcome The Deficiencies

As discussed above in Section A and Section B.1., the asserted combination of the '525 and '107 references fails to consider the asserted references "as a whole", contrary to the requirements of M.P.E.P. § 2142.02, and fails to support any proper reason for the asserted modification of the teachings of the '525 reference. Now taking into account the '251 reference, the same above-noted deficiencies are present. Nothing in the '251 reference has been cited to teach that the properties of a metal gate electrode are applicable to a silicon activated region in any regards that would address the problems noted, e.g., as discussed in connection with the '107 reference. Accordingly, the § 103(a) rejection of claims 8 and 18-19 is improper for the reasons set forth above in Section A.

For the reasons above, Appellant submits that the § 103(a) rejection of claims 8, 18 and 19 is improper, and requests that the rejection be reversed.

C. The § 103(a) Rejection Of Claim 9 Is Improper Because The '525 Reference Teaches Away From The Asserted Combination.

Appellant has explained that the combination is improper because the '525 reference teaches away from the claim 9 limitation regarding an amorphous upper gate, and the Examiner has not provided any substantive response. The '525 reference teaches that the final gate structure should have a crystalline silicon upper gate and even explains that if amorphous material is used in the process, it should be converted to crystalline material. In attempting to provide a response, the Examiner merely restates what aspects of the references are relied upon for the rejection; the Examiner does not, however, provide any rebuttal of Appellant's explanation that would render the '525 reference unsatisfactory for restraining the diffusion of Ge through the grain boundary. A careful review of the Examiner's response in this regard reveals that the Examiner has failed even to acknowledge the intended operation of the primary '525 reference – which is the core point of Appellant's argument. Accordingly, the record stands uncontroverted in showing that the '525 reference teaches away from the proposed modification of the '525 reference.

Consistent with the above-cited *KSR* decision, M.P.E.P. § 2143.01 explains the long-standing principle that a § 103 rejection cannot be maintained when the asserted modification undermines either the operation or the purpose of the main ('525) reference - the rationale being that the prior art teaches away from such a modification. *See KSR* at 1742 ("[W]hen the prior art teaches away from combining certain known elements, discovery of a successful means of combining them is more likely to be non-obvious."). Accordingly, evidence of teaching away from a proposed modification is strong evidence of non-obviousness.

More specifically, the proposed modification is contrary to the '525 reference's restraining the diffusion of Ge through the grain boundary from the lower layer 23 to the upper layer 24 by giving the lower layer 23 a columnar crystalline structure and the upper layer 24 random crystalline structure. *See, e.g.,* Col. 4:50 to Col. 5:22 and Figure 3. The '525 reference expressly teaches that in order to provide the appropriate restraint to the diffusion of Ge, an amorphous silicon layer is crystallized. As explicitly described in the description of the formation of the structure in cited Figure 3, if the upper layer is intermediately formed from amorphous silicon during manufacture (as proposed), "the amorphous Si layer is [then] crystallized to have a random polycrystalline structure . . . [c]onsequently, the formed gate structure is the same as that shown in Figure 3." *See, e.g.,* Col. 5:41-44. The record teaches that amorphous silicon renders the device of the '525 reference unsatisfactory for restraining the diffusion of Ge through the grain boundary. By the Examiner's proposed modification, however, the resulting gate includes an amorphous silicon layer that does not adequately restrain the diffusion of Ge as required by the '525 reference. Therefore, the '525 reference teaches away from the proposed structure and there is no motivation for the skilled artisan to modify the '525 reference in the manner proposed by the Examiner.

Accordingly, the § 103(a) rejection of claim 9 is improper and Appellant requests that it be reversed.

VIII. Conclusion

In view of the above, Appellant submits that the rejections of claims 6-14 and 17-24 are improper and therefore requests reversal of the rejections as applied to the appealed claims and allowance of the entire application.

Authority to charge the undersigned's deposit account was provided on the first page of this brief.

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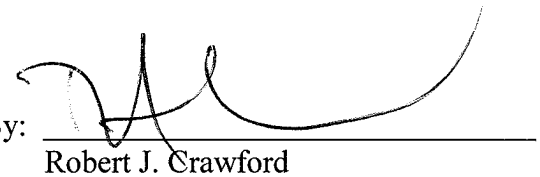
By: 

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APPENDIX OF CLAIMS INVOLVED IN THE APPEAL
(S/N 10/550,741)

6. An MIS type semiconductor device, comprising:

a semiconductor substrate,

a gate electrode formed on a gate insulating film and formed of gate material,

wherein the gate electrode comprises:

a first layer of activated crystalline gate material having a first side oriented towards the substrate and in contact with the gate insulating film, a second side oriented away from the substrate and a grain size, the first layer of activated crystalline gate material having a doping level of 10^{19} ions/cm^3 or higher, and

a second layer of gate material in contact with the first layer of activated crystalline gate material at the second side of the first layer of activated crystalline gate material, the second layer of gate material having a grain size,

wherein the grain size of the second layer of gate material is at least twice as large as the grain size of the first layer of activated crystalline gate material.

7. A semiconductor device according to claim 6, wherein the first layer of activated crystalline gate material has a doping level of about 10^{20} ions/cm^3 or higher.

8. An MIS type semiconductor device according to claim 6, wherein

a doping implant in the activated gate material has an abruptness of a doping profile of about 2 nm or more.

9. A semiconductor device according to claim 6, wherein the second layer of gate material consists of amorphous gate material.

10. A semiconductor device according to claim 6, wherein the second layer of gate material consists of polycrystalline gate material.

11. A semiconductor device according to claim 6, wherein the grain size in the second layer is below about 40 nm.

12. A semiconductor device according to claim 6, wherein the first layer is crystalline or very fine-grained, with grains below 5 nm.

13. A semiconductor device according to claim 6, wherein the gate insulating film is provided between the semiconductor substrate and the gate electrode.

14. A semiconductor device according to claim 6, wherein the device is a transistor.

17. A semiconductor device according to claim 6, wherein the first layer of activated crystalline gate material has a doping level of about 5×10^{20} ions/cm^3 or higher.

18. An MIS type semiconductor device according to claim 6, wherein

a doping implant in the activated gate material has an abruptness of a doping profile of about 1.5 nm or more.

19. An MIS type semiconductor device according to claim 6, wherein

a doping implant in the activated gate material has an abruptness of a doping profile of about 1 nm.

20. A semiconductor device according to claim 6, wherein the grain size in the second layer is below about 30 nm.

21. A semiconductor device according to claim 6, wherein the grain size of the second layer of gate material is about six times as large as the grain size of the first layer of activated crystalline gate material.

22. A semiconductor device according to claim 6, wherein the grain size of the first layer of activated crystalline gate material reduces gaps between the first layer of activated crystalline gate material and the gate insulating film.

23. A semiconductor device according to claim 6, wherein the first layer of activated crystalline gate material is silicon.

24. An MIS type semiconductor device, comprising:

a semiconductor substrate;

a gate insulating film formed on the substrate; and

a gate electrode formed on the gate insulating film, the gate electrode including:

a first layer of activated crystalline gate material having a first side oriented towards the substrate and in contact with the gate insulating film, a second side oriented away from the substrate and a grain size of less than about 5nm, the first layer of activated crystalline gate material having a doping level of 10^{19} ions/cm^3 or higher, and

a second layer of gate material in contact with the first layer of activated crystalline gate material at the second side of the first layer of activated crystalline gate material, the second layer of gate material having a grain size of less than about 40 nm,

wherein the grain size of the first layer of activated crystalline gate material is smaller than the grain size of the second layer of gate material.

APPENDIX OF EVIDENCE

Appellant is unaware of any evidence submitted in this application pursuant to 37 C.F.R. §§ 1.130, 1.131, and 1.132.

APPENDIX OF RELATED PROCEEDINGS

As stated in Section II above, Appellant is unaware of any related appeals, interferences or judicial proceedings.